

Remarks

In an interview with the Examiner held on February 15, 2007, agreement was reached that addition of the limitation “wherein the plurality of demodulators recover a plurality of bits synchronously distributed across the plurality of transmission bands in the serial/deserializer transmission system” to claim 7, and addition of the limitation “wherein the plurality of bits synchronously transmitted across the plurality of transmission bands of the serial/deserializer system is recovered” added to claims 38 and 45 would make those claims allowable over the cited prior art. An Amendment after Final was then filed on February 21, 2007, which amended the claims in the way discussed during the interview.

In an Advisory Action mailed on March 21, 2007, the Examiner commented that “[t]he amendments raise an issue of new matter, as there appears to be no support in the specification for synchronously transmitted/distributed bits.” These remarks address that issue raised by the Examiner.

The Synchronous nature of the Applicant’s invention is taught throughout the specification. The Abstract, for example, discloses that “N-bit parallel data is transmitted in K-frequency separated channels on the transmission medium so as to fully take advantage of the overall bandwidth of the transmission medium.” This necessarily indicates, in itself, a synchronous system.

Figures 2B and 2C, as another example, shows utilization of a single reference clock (REF CK) input to both the transmitter portion and the receiver portion of Applicant’s described system. As indicated in Figure 2C, each of the demodulators works on the same reference clock to retrieve the N parallel bits of data from the frequency separated channels demodulated by

demodulators 222-1 through 222-K. Again, an explicit teaching of a synchronous system for retrieving bits from the plurality of transmission bands.

Figure 4 illustrates a single one of the transmission modulators, and operates from the reference clock signal input to all of the modulators as shown in Figure 2B. Figure 5 illustrates a single one of the receive demodulators, and indicates a PLL 523 which “can be a free-running loop generating clock signals for receiver 222-k based on the reference clock signal.” Par. [0075]. Therefore, all of the demodulators run from the same reference clock, indicating synchronous receipt of the bits in each of the frequency separated channels.

As further indication of synchronous behavior, in Paragraph [0070] the specification discloses that all of the baud rates for all of the frequency separated channels can be the same: “[i]n some embodiments, B_k and γ_k can be the same for all channels” This in particular describes synchronous systems where each channel carries the same baud rate and the parallel bits of data are allocated amongst the various channels. Further, in Paragraph [0072], the particular examples provided are all for fully synchronous systems.

Further, paragraphs [0074] and [0075] discuss adjustment of clock frequency and phase in order to adjust for the event where the transmitter clock frequency and the receiver clock frequency are slightly different. This consideration, in itself, indicates a teaching of a synchronous system where the bits of data received on the plurality of frequency separated channels are synchronously received into parallel bits of data.

Therefore, throughout the specification of the application, it is clear that a synchronously transmitted and distributed bits are taught. Applicants are filing a Request for Continued Application along with these remarks and request that the Examiner enter the previously filed amendment and provide a Notice of Allowability for the pending claims. If the Examiner

contemplates other action, or if the Examiner has any questions regarding these Remarks, the Examiner is invited to contact Applicant's attorney at 650-849-6622.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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